Ordering number : ENA0017

SANYO Semiconductors
DATA SHEET

LA76850 — Monolithic Linear IC Black & White Television IC

Overview

LA76850 is a Black & White Television IC.

Functions

- I^2C Bus Control VIF/SIF/Y/Deflection/Implemented in a Single Chip

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_8 max		7.0	V
	V_{27} max		7.0	V
Maximum supply current	I16 max		14	V
	I_{20} max		35	V
Allowable power dissipation	Pd max	Ta ≤ 65°C *	1.1	mW
Operating temperature	Topg		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C

* Provided with a glass epoxy board (114.3×76.1×1.6 mm)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_8		5.0	V
	V_{27}		5.0	V
Recommended supply current	I_{16}		9	mA
	I_{20}		29	mA
Operating supply voltage range	V_8 op		4.7 to 5.3	V
	V_{27} op		4.7 to 5.3	V
Operating supply current range	I_{16} op		7 to 11	mA
	I_{20} op		24 to 33	mA

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Electrical Characteristics Ta = 25°C, $V_{CC}L = V_8 = V_{27} = 5.0V$, $I_{CC} = I_{16} = 9mA$, $I_{CC} = I_{20} = 27mA$

Parameter	Symbol	Conditions	min	typ	max	unit
[Circuit voltage, current]						
IF supply current	I_8	V_8 = 5V, V_3 = 2.5V		67		mA
RGB supply voltage	V_{16}	I_{16} = 9mA		8.0		V
Horizontal supply voltage	V_{20}	I_{25} = 27mA		5.0		V
Video supply current	I_{27}	I_{27} = 5V		65		mA
[VIF block]						
Maximum RFAGC voltage	VRFH	CW = 80dBμ, DAC = 0	8.5	9		Vdc
Minimum RFAGC voltage	VRFL	CW = 80dBμ, DAC = 63	0	0.3	0.7	Vdc
RF AGC Delay Pt (@DAC = 0)	RFAGC0	DAC = 0	90			dBμ
RF AGC Delay Pt (@DAC = 63)	RFAGC63	DAC = 63			80	dBμ
Input sensitivity	Vi	Output-3dB			46	dBμ
No-signal video output voltage	VOn	No signal	3.4	3.7	4.0	Vdc
Sync signal tip level	VOtip	CW = 80dBμ	1.1	1.4	1.7	Vdc
Video output amplitude	VO	80dBμ, AM = 78%, fm = 15kHz	1.57	2.05	2.52	Vp-p
Video S/N	S/N	CW = 80dBμ	40	45		dB
C-S beat level	IC-S	V4.43MHz/V1.07MHz	35			dB
Differential gain	DG	80dBμ, 87.5% Video MOD		5.0	10.0	%
Differential phase	DP	80dBμ, 87.5% Video MOD		1.0	10.0	deg
Maximum AFT output voltage	VAFTH	CW = 80dBμ, frequency variations	4.3	4.7	5	Vdc
Minimum AFT output voltage	VAFTL	CW = 80dBμ, frequency variations	0.0	0.3	0.7	Vdc
AFT detection sensitivity	VAFTS	CW = 80dBμ, frequency variations	8.0	15.0	22.0	mV/kHz
APC pull-in range (U)	fPU		1.5			MHz
APC pull-in range (L)	fPL		1.5			MHz
NT Trap1 (4.5MHz)	NTR1				-30	dB
NT Trap1 (4.8MHz)	NTR2				-20	dB
BG Trap1 (5.5MHz)	BTR1				-30	dB
BG Trap2 (5.85MHz)	BTR2				-20	dB
I Trap1 (6.0MHz)	ITR1				-30	dB
I Trap1(6.55MHz)	ITR2				-17	dB
DK Trap1(6.5MHz)	DTR1				-30	dB
[SIF block]						
FM detection output voltage	SOADJ	FM = ±30kHz	245	310	390	mVrms
FM limiting sensitivity	SLS	Output -3dB			53	dBμ
FM detection output f characteristics	SF	fm = 100kHz	-0.5	5.0	8.0	dB
FM detection output distortion	STHD	FM = ±30kHz			1.0	%
AM rejection ratio	SAMR	AM = 30%	40			dB
SIF S/N	SSN	DIN.Andio	51.5			dB
PAL de-emph time constant	SPTC		2.4	3.0	3.6	dB
PAL/NT Difference of voltage gain	SGD		-1.5	0.0	+1.5	dB
NT de-emph time constant	SNTC		1.9	2.5	3.1	dB

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Parameter	Symbol	Conditions	min	typ	max	unit
[AUDIO block]						
Maximum gain	AGMAX	1kHz500mVrms	-2.0	0.5	+3.0	dB
Variable range	ARANGE		60	74		dB
Frequency characteristics	AF	20kHz	-3.0	0.0	3.0	dB
Mute	AMUTE	20kHz	70			dB
Distortion	ATHD	1kHz, 500mVrms, Vol: MAX			0.5	%
S/N	ASN	DIN. Audio	65	73		dB
Crosstalk	ACT	1kHz	70			dB
[Video block]						
Video signal input 1DC voltage	V_{IN}1DC		2.2	2.5	2.8	V
Video signal input 1AC voltage	V_{IN}1AC			1		Vp-p
Video overall gain (Contrast max)	CONT127		12.0	14.0	16.0	dB
Contrast adjustment characteristics (Normal/max)	CONT63		-6.5	-5.0	-3.5	dB
Contrast adjustment characteristics (Min/max)	CONT0		-18.0	-15.0	-12.0	dB
Video frequency Characteristics 1 NTSC	BW1	1.8MHz/100kHz Filter sys = 0000	-6.0	-3.0	0.0	dB
Video frequency characteristics 2 PAL	BW2	2.2MHz/100kHz Filter sys = 0010	-6.0	-3.0	0.0	dB
Chroma trap amount PAL	CtrapP		-36.0	-26.0	-22.0	dB
Chroma trap amount NTSC	CtrapN		-36.0	-26.0	-22.0	dB
DC transmission amount	ClampG1		95.0	100.0	105.0	%
Sharpness variability range (trap 2 mid) (trap 2 max) (trap 2 min)	Sharp32T2	F = 2.7MHz, FILTER SYS = 0010	5.0	8.0	11.0	dB
	Sharp63T2	F = 2.7MHz, FILTER SYS = 0010	8.5	11.5	13.5	dB
	Sharp0T2	F = 2.7MHz, FILTER SYS = 0010	-6.5	-3.5	-0.5	dB
	Sharp63T5	F = 3.0MHz, FILTER SYS = 0000 Y APF = 1	8.5	11.5	13.5	dB
	Sharp0T5	F = 3.0MHz, FILTER SYS = 0000 Y APF = 1	-6.5	-3.5	-0.5	dB
Y gamma effective point 1	YG1	YGAMMA = 01	89.0	93.0	97.0	%
Y gamma effective point 2	YG2	YGAMMA = 10	85.0	89.0	93.0	%
Y gamma effective point 3	YG3	YGAMMA = 11	80.0	84.0	88.0	%
Horizontal/vertical blanking output level	RGBBLK		0.1	0.4	0.7	V
[OSD block]						
OSD Fast SW threshold	FSTH		0.7	0.9	1.1	V
OSD output level	OSDH	Digital osd = 1 Osd cont = 63	140	175	210	IRE
[RGB output (cutoff drive) block]						
Brightness control (Normal)	BRT63		2.3	2.8	3.3	V
Brightness control (Normal-H)	BRT63H		3.0	3.3	3.6	V
Hi brightness (max)	BRT127		20	25	30	IRE
Low brightness (min)	BRT0		-30	-25	-20	IRE
Bright control Resolution	Vbiassns			16		mV /Bit
Sub-bias control Resolution	Vsbiassns			7		mV /Bit

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Parameter	Symbol	Conditions	min	typ	max	unit
[Deflection block]						
Horizontal free-running frequency	FH		15500	15670	15900	Hz
Horizontal pull-in range	fH PULL		±400			Hz
Horizontal output pulse width	Hduty		36.1	37.6	39.1	µs
Horizontal output pulse saturation voltage	V Hsat		0	0.2	0.4	V
Vertical free-running cycle 50	VFR50		312.0	312.5	313.0	H
Vertical free-running cycle 60	VFR60		262.0	262.5	263.0	H
Horizontal output pulse phase	HPHCENpal		9.5	10.5	11.5	µs
Horizontal output pulse phase	HPHCENnt		9.5	10.5	11.5	µs
Horizontal position adjustment range	HPHrange	5bit		±2.4		µs
Horizontal position adjustment maximum variability width	HPHstep				350.0	ns
Horizontal blanking left @0	BLKL0	BLKL:000	7500	8300	9100	ns
Horizontal blanking left @7	BLKL7	BLKL:111	10800	11600	12400	ns
Horizontal blanking right @0	BLKR0	BLKR:000	1800	2600	3400	ns
Horizontal blanking right @7	BLKR7	BLKR:111	-1100	-300	500	ns
Sand castle pulse crest value H	SANDH		5.3	5.6	5.9	V
Sand castle pulse crest value M1	SANDM1		3.7	4.0	4.3	V
Sand castle pulse crest value M2	SANDM2		1.7	2.0	2.3	V
Sand castle pulse crest value L	SANDL		0.1	0.4	0.7	V
Burst gate pulse width	BGPWD		2.5	3.0	3.5	µs
Burst gate pulse phase	BGPPH		4.9	5.4	5.9	µs
Horizontal output stop voltage	Hstop		3.30	3.60	3.90	V
<Vertical screen size adjustment>						
Vertical ramp output amplitude PAL@64	Vspal64	VSIZE: 1000000	0.85	0.95	1.05	Vp-p
Vertical ramp output amplitude NTSC@64	Vsnt64	VSIZE: 1000000	0.85	0.95	1.05	Vp-p
Vertical ramp output amplitude PAL@0	Vspal0	VSIZE: 0000000	0.41	0.51	0.61	Vp-p
Vertical ramp output amplitude NTSC@0	vsnt0	VSIZE: 0000000	0.41	0.51	0.61	Vp-p
Vertical ramp output amplitude PAL@127	Vspal127	VSIZE: 1111111	1.15	1.30	1.45	Vp-p
Vertical ramp output amplitude NTSC@127	Vspal127	VSIZE: 1111111	1.15	1.30	1.45	Vp-p

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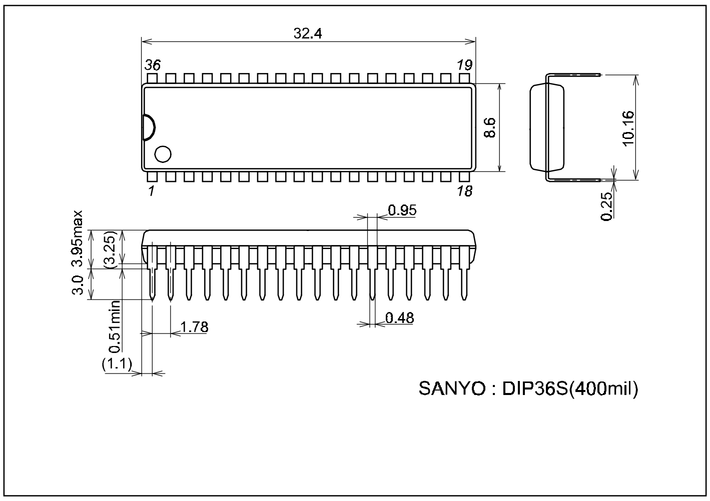
Parameter	Symbol	Conditions	min	typ	max	unit
<High-voltage dependent vertical size correction>						
Vertical size correction @0	Vsizecomp	VCOMP: 000	0.89	0.93	0.97	ratio
<Vertical screen position adjustment>						
Vertical ramp DC voltage PAL@32	Vdcpal32	VDC: 100000	2.25	2.40	2.55	Vdc
Vertical ramp DC voltage NTSC@32	Vdcnt32	VDC: 100000	2.25	2.40	2.55	Vdc
Vertical ramp DC voltage PAL@0	Vdcpal0	VDC: 000000	1.85	2.00	2.15	Vdc
Vertical ramp DC voltage NTSC@0	Vdcpal0	VDC: 000000	1.85	2.00	2.15	Vdc
Vertical ramp DC voltage PAL@63	Vdcpal63	VDC: 111111	2.65	2.80	2.95	Vdc
Vertical ramp DC voltage NTSC@63	Vdcpal63	VDC:111111	2.65	2.80	2.95	Vdc
Vertical linearity @16	Vlin16	VLIN: 10000	0.85	1.00	1.15	ratio
Vertical linearity @0	Vlin0	VLIN: 00000	1.17	1.32	1.47	ratio
Vertical linearity @31	Vlin31	VLIN: 11111	0.57	0.72	0.87	ratio
Vertical S-shaped correction @16	Vscor16	VSC: 10000	0.75	0.90	1.05	ratio
Vertical S-shaped correction @0	Vscor0	VSC: 00000	1.08	1.23	1.38	ratio
Vertical S-shaped correction @31	Vscor31	VSC: 11111	0.49	0.64	0.79	ratio

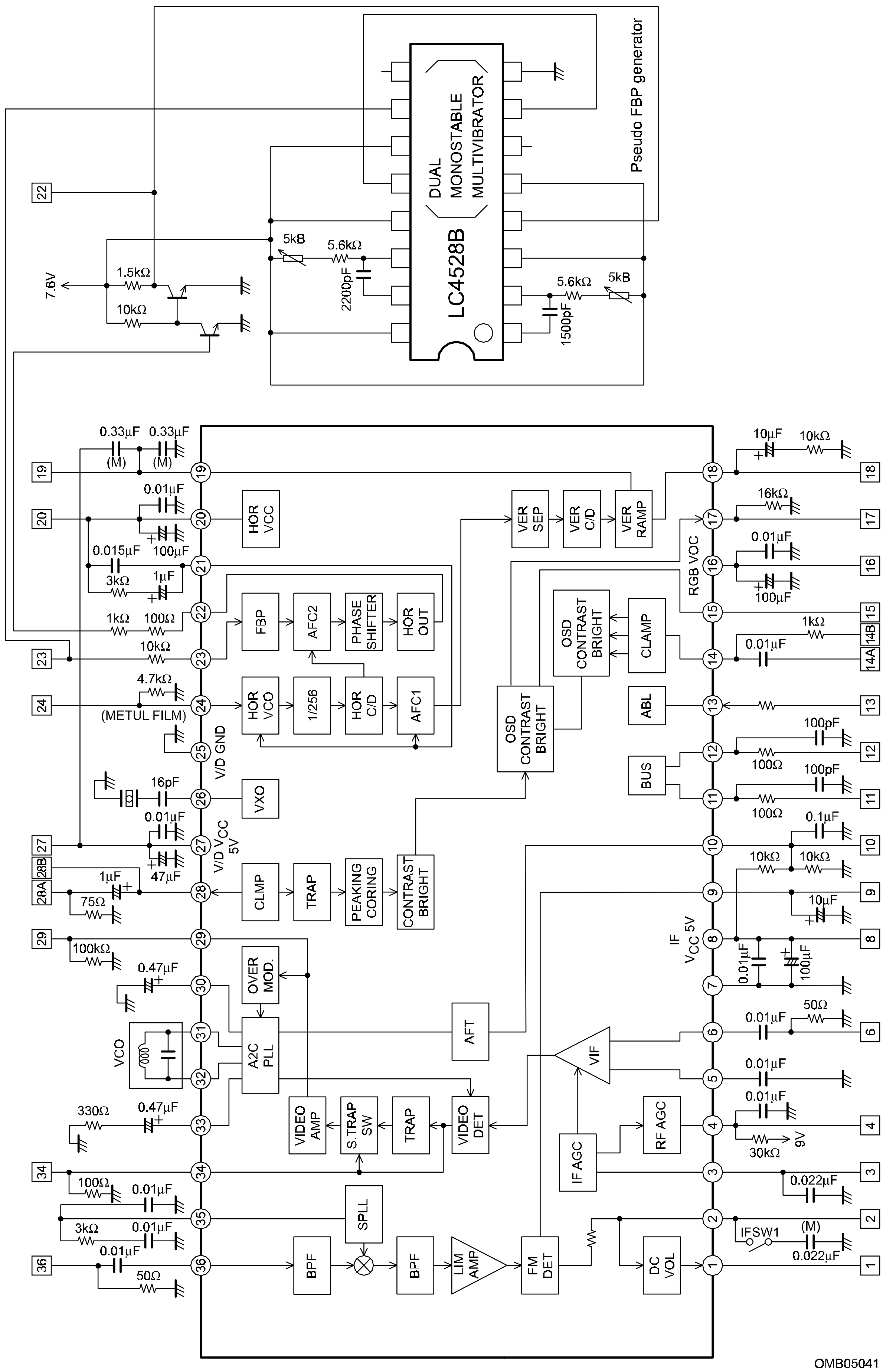
Package Dimensions

unit : mm

3170A



Application Circuit Example

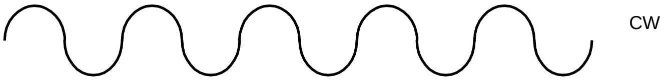
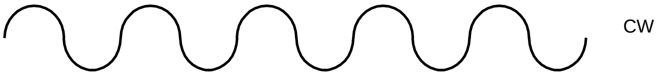
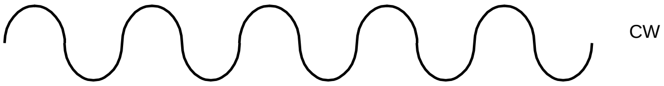
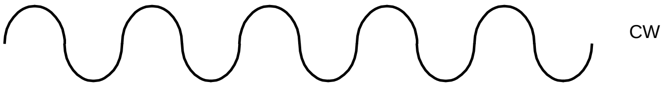
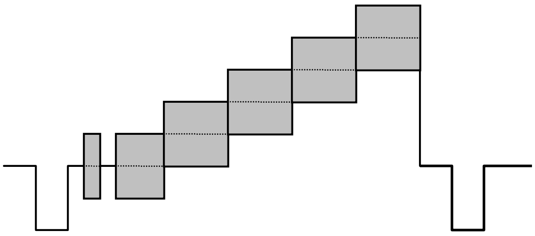
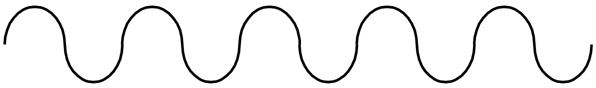
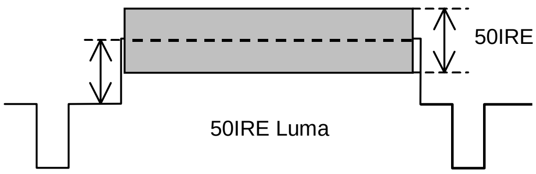


Test Conditions Ta = 25°C, $V_{CC} = V_8 = V_{31} = V_{43}$ = 5.0V, l_{18} = 19mA, $I_{CC} = l_{25}$ = 27mA

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Circuit voltage, current]					
RGB supply voltage (pin 20)	V_{20}	(20)	No signal	Apply a current of 27mA to pin 20 and measure the voltage at pin 20.	Initial
RGB supply voltage (pin 16)	V_{16}	(16)	No signal	Apply a current of 19mA to pin 16 and measure the voltage at pin 16.	Initial
IF supply current (pin 8)	I_8 ($CDDI_{CC}$)	[8]	No signal	Apply a voltage of 5.0V to pin 8 and measure the incoming DC current (mA). (IF AGC 2.5V applied)	Initial
Video/vertical supply current (pin 27)	I_{27} ($DEFI_{CC}$)	[27]	No signal	Apply a voltage of 5.0V to pin 27 and measure the incoming DC current (mA).	Initial

VIF Block   Input Signals

1. Input signals must all be input to the PIF IN (pin 6) in the Test Circuit.
2. All input signal voltage values are the levels at the VIF IN (pin 6) in the Test Circuit.
3. Signal contents and signal levels
4. Bus conditions: VIF SYS = "01", S.TRAP.SW = "1", OVER.MOD.SW = "0"

Input signal	Waveform	Conditions
SG1		38.9MHz
SG2		34.47MHz
SG3		33.4MHz
SG4		Frequency variable
SG5		38.9MHz 87.5% Video Mod. 10-stairstep wave (Subcarrier: 4.43MHz)
SG6		38.9MHz fm = 15kHz, AM = 78%
SG7		38.9MHz, 80dBμ 87.5% Video Mod. 50IRE Luma (Carrier: variable)

VIF Block Test Conditions

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Maximum RF AGC voltage	VRFH	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF.AGC = "000000"
Minimum RF AGC voltage	VRFL	4	SG1 80dBμ	Measure the DC voltage at pin 4.	RF.AGC = "111111"
RF AGC Delay Pt (@DAC = 0)	RFAGC0	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF.AGC = "000000"
RF AGC Delay Pt (@DAC = 63)	RFAGC63	4	SG1	Obtain the input level at which the DC voltage at pin 4 becomes 4.5V.	RF.AGC = "111111"
Input sensitivity	Vi	29	SG6	Using an oscilloscope, observe the level at pin 29 and obtain the input level at which the waveform's p-p value becomes 1.4Vp-p.	
No-signal video output voltage	VOn	29	No signal	Set IF AGC = “1” and measure the DC voltage at pin 29.	
Sync signal tip level	VOtip	29	SG1 80dBμ	Measure the DC voltage at pin 29.	
Video output amplitude	VO	29	SG6 80dBμ	Using an oscilloscope, observe the level at pin 29 and measure the waveform’s p-p value.	
Video S/N	S/N	29	SG1 80dBμ	Measure the noise voltage (Vsn) at pin 29 with an RMS voltmeter through a 10kHz to 5.0MHz band-pass filter and calculate 20 log (1.43/Vsn).	
C-S beat level	IC-S	29	SG1 SG2 SG3	Input a 80dBμ SG1 signal and measure the DC voltage (V3) at pin 3. Mix SG1 = 74dBμ, SG2 = 64 dBμ, and SG3 = 64 dBμ to enter the mixture in the VIF IN. Apply V3 to pin 3 from an external DC power supply. Using a spectrum analyzer, measure the difference between pin 29’s 4.43MHz component and 1.07MHz component.	
Differential gain	DG	29	SG5 80dBμ	Using a vector scope, measure the level at Pin 29.	
Differential phase	DP	29	SG5 80dBμ	Using a vector scope, measure the level at Pin 29.	
Maximum AFT output voltage	VAFTH	10	SG4 80dBμ	Set and input the SG4 frequency to 37.9MHz to be input. Measure the DC voltage at pin 10 at that moment.	
Minimum AFT output voltage	VAFTL	10	SG4 80dBμz	Set and input the SG4 frequency to 39.9MHz to be input. Measure the DC voltage at pin 10 at that moment.	
AFT detection sensitivity	VAFTS	10	SG4 80dBμz	Adjust the SG4 frequency and measure frequency deviation Δf when the DC voltage at pin 10 changes from 1.5V to 3.5V. VAFTS = 2000/Δf [mV/kHz]	

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Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
APC pull-in range (U), (L)	fPU, fPL	29	SG4 80dBµ	Connect an oscilloscope to pin 29 and adjust the SG4 frequency to a frequency higher than 38.9MHz to bring the PLL into unlocked mode. (A beat signal appears.) Lower the SG4 frequency and measure the frequency at which the PLL locks again. In the same manner, adjust the SG4 frequency to a lower frequency to bring the PLL into unlocked mode. Higher the SG4 frequency and measure the frequency at which the PLL locks again.	
NT Trap1 (4.5MHz), 2 (4.8MHz)	NTR1 NTR2	29	SG7	Determine the output level difference between carrier frequencies of 1Mhz, 4.5MHz and 4.8MHz. (Reference:1MHz)	SIF.SYS = "00"
BG Trap1 (5.5MHz), 2 (5.85MHz)	BTR1 BTR2	29	SG7	Determine the output level difference between carrier frequencies of 1Mhz, 5.5MHz and 5.85MHz. (Reference:1MHz)	SIF.SYS = "01"
I Trap1 (6.0MHz) 2 (6.55MHz)	ITR1 ITR2	29	SG7	Determine the output level difference between carrier frequencies of 1MHz, 6.0MHz and 6.55MHz. (Reference:1MHz)	SIF.SYS = "10"
DK Trap1 (6.5MHz)	DTR1	29	SG7	Determine the output level difference between carrier frequencies of 1MHz and 6.5MHz. (Reference:1MHz)	SIF.SYS = "11"

SIF Block (FM block) Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition:
   IF.AGC.SW = "1", SIF.SYS = "01", DEEM-TC = "0", FM.GAIN = "0", A.MONI.SW = "0", A2.SW = "0"
2. SW:IF1 = "ON", 24pin = 5V
3. Input signals are input to pin 54 and the carrier frequency is 5.5MHz.

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
FM detection output voltage	SOADJ	2	90dBµ, fm = 400Hz, FM = ±30kHz	Measure the 400 Hz component (SV1: mVrms) of the FM detection output at pin 2.	
FM limiting sensitivity	SLS	2	fm = 400Hz, FM = ±30kHz	Measure the input level (dBµ) at which the 400Hz component of the FM detection output at pin 2 becomes -3dB relative to SV1.	
FM detection output f characteristics (fm=100kHz)	SF	2	90dBµ, fm = 100kHz FM = ±30kHz	Set SW: IF1 = "OFF". Measure (SV2: mVrms) the FM detection output of pin 2. Calculate as follows: SF = 20*LOG (SV1/SV2) [dB]	
FM detection output distortion	STHD	2	90dBµ, fm = 400Hz, FM = ±30kHz	Measure the distortion factor of the 400Hz component of the FM detection output at pin 2.	
AM rejection ratio	SAMR	2	90dBµ, fm = 400Hz, AM = 30%	Measure the 400Hz component (SV3: mVrms) of the FM detection output at pin 2. Assign the measured value to SV3 and calculate as follows: SAMR = 20*log (SV1/SV3) [dB]	
SIF.S/N	SSN	2	90dBµ, CW	Measure the noise level (DIN AUDIO, SV4: mVrms) at pin 2. Calculate as follows: SSN=20*log(SV1/SV4) [dB]	
PAL de-emph time constant	SPTC	2	90dBµ, fm = 3.18KHz FM = ±30KHz	Measure the 3.18kHz component (SV5: mVrms) of the FM detection output at pin 2 and calculate as follows: SNTC = 20*LOG (SV1/SV5) [dB]	
PAL/NT Difference of voltage gain	SGD	2	fo = 4.5MHz 90dBµ, fm = 400Hz FM = ±15KHz	Measure the 400Hz component (SV6: mVrms) of the FM detection output at pin 2 and calculate as follows: SNTC = 20*LOG (SV1/SV6) [dB]	SIF.SYS = "00" DEEM-TC = "1" FM.GAIN = "1"
NT de-emph time constant	SNTC	2	fo = 4.5MHz 90dBµ, fm = 2.12kHz FM = ±15kHz	Measure the 2.12kHz component (SV7: mVrms) of the FM detection output at pin 2 and calculate as follows: SNTC = 20*LOG (SV6/SV7) [dB]	SIF.SYS = "00" DEEM-TC = "1" FM.GAIN = "1"

Audio Block Input Signals and Test Conditions

Unless otherwise specified, the following conditions apply when each measurement is made.

1. Bus control condition:
   AUDIO.MUTE = "0", A.MONI.SW = "0", AUDIO.SW = "1", VOL.FIL = "0", SIF.SYS = "01", IF.AGC.SW = "1"
2. Input 5.5MHz, 90dBμ and CW at pin 54.
3. Enter an input signal from pin 51.

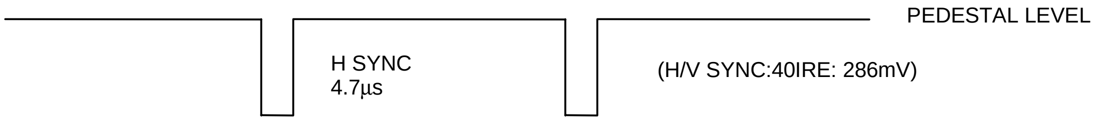
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Maximum gain	AGMAX	1	1kHz, CW 500mVrms	Measure the 1kHz component (V1: mVrms) at the pin 1 and calculate as follows: AGMAX = 20*LOG(V1/500) [dB]	VOLUME = "1111111"
Variable range	ARANGE	1	1kHz, CW 500mVrms	Measure the 1kHz component (V2: mVrms) at the pin 1 and calculate as follows: ARANGE = 20*LOG(V1/V2) [dB]	VOLUME = "0000000"
Frequency characteristics	AF	1	20kHz, CW 500mVrms	Measure the 20kHz component (V3: mVrms) at the pin 1 and calculate as follows: AF = 20*Log(V3/V1) [dB]	VOLUME = "1111111"
Mute	AMUTE	1	20kHz, CW 500mVrms	Measure the 20kHz component (V4: mVrms) at the pin 1 and calculate as follows: AMUTE = 20*Log(V3/V4) [dB]	VOLUME = "1111111" AUDIO.MUTE = "1"
Distortion	ATHD	1	1kHz, CW 500mVrms	Measure the distortion of the 1kHz component at the pin 1.	VOLUME = "1111111"
S/N	ASN	1	No signal	Measure the noise level (DIN AUDIO, V5: mVrms) at the pin 1 and calculate as follows: ASN = 20*log(V1/V5) [dB]	VOLUME = "1111111"
Crosstalk	ACT	1	1kHz, CW 500mVrms	Measure the 1kHz component (V6: mVrms) at the pin 1 and calculate as follows: ACT = 20*LOG(V1/V6) [dB]	VOLUME = "1111111" AUDIO.SW = "0"

Video Block Input Signals

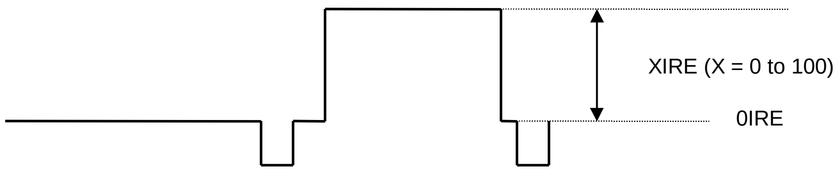
Y IN input signal 100IRE: 714mV

Bus control bit conditions: Initial test state

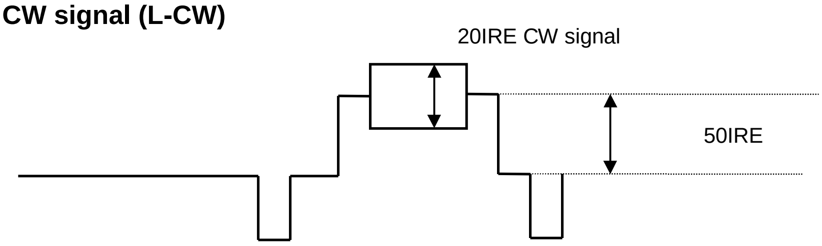
0IRE signal (L-0): NTSC standard sync signal



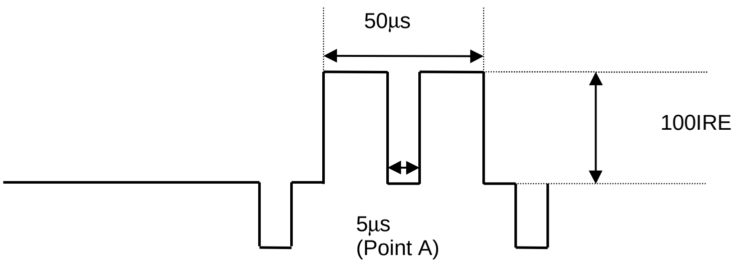
XIRE signal (L-X)



CW signal (L-CW)

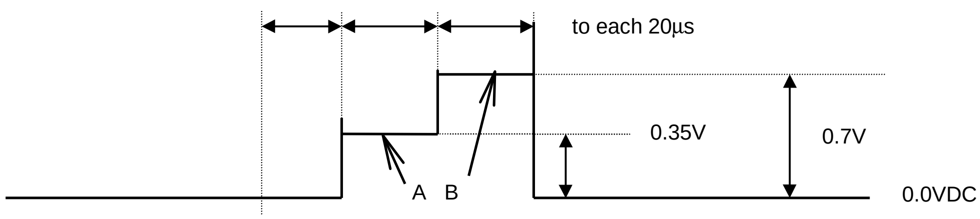


BLACK STRETCH 0IRE signal (L-BK)

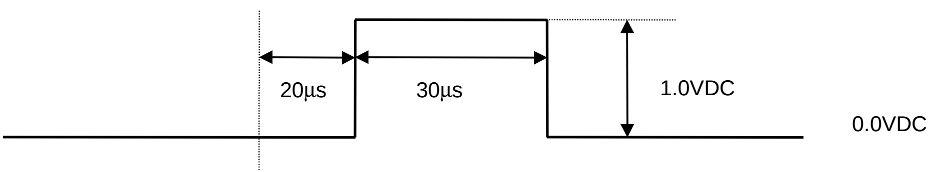


OSD IN Input signal

OSD Input signal 1 (0-1)



OSD Input signal 2 (0-2)



Video Block Test Conditions

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Video signal input 1DC voltage	V_{IN}1DC	28	L-100	Input signals to pin 28 and measure the voltage of the pedestal.	VIDEO SW:1
Video signal input 1 AC voltage	V_{IN}1AC	28		Pin 28 recommended input level	
Video overall gain (Contrast max)	CONT127	17	L-50	Measure the output signal's 50IRE amplitude (CNTHB Vp-p) and calculate CONT127 = 20log (CNTHB/0.357).	CONTRAST: 1111111
Contrast adjustment characteristics (normal/max)	CONT63	17	L-50	Measure the output signal's 50IRE amplitude (CNTCB Vp-p) and calculate CONT63 = 20log (CNTCB/0.357).	CONTRAST: 0111111
Contrast adjustment characteristics (min/max)	CONT0	17	L-50	Measure the output signal's 50IRE amplitude (CNTLB Vp-p) and calculate CONT0 = 20log (CNTLB/0.357).	CONTRAST: 0000000
Video frequency Characteristics 1 (NTSC)	BW1	17	L-CW	With the input signal's continuous Wave = 100kHz, measure the output signal's continuous wave amplitude (PEAKDC Vp-p). With the input signal's continuous wave = 1.8MHz, measure the output signal's continuous wave amplitude (CW1.8 Vp-p). Calculate BW1 = 20Log (CW1.8/PEAKDC).	FILTER SYS: 0000 SHARPNESS: 000000
Video frequency Characteristics 2 (PAL)	BW2	17	L-CW	With the input signal's continuous wave = 2.2MHz, measure the output signal's continuous wave amplitude (CW2.2 Vp-p). Calculate BW2 = 20Log (CW2.2/PEAKDC).	FILTER SYS: 0010 SHARPNESS: 000000
Chroma trap amount PAL	CtraPP	17	L-CW	With the input signal's continuous wave = 4.43MHz, measure the output signal's continuous wave amplitude (F0P Vp-p). Calculate CtraP = 20Log (F0P/PEAKDC).	FILTER SYS: 010 Sharpness: 000000
Chroma trap amount NTSC	CtraPN	17	L-CW	With the input signal's continuous wave = 3.58MHz, measure the output signal's continuous wave amplitude (F0N Vp-p). Calculate CtraN = 20Log (F0N/PEAKDC).	FILTER SYS: 000 Sharpness: 000000
DC transmission amount	ClampG1	17	L-0	Measure the output signal's 0IRE DC level (BRTPL V).	Brightness: 0000000 CONTRAST: 1111111
			L-100	Measure the output signal's 0IRE DC level (DRVPH V) and 100IRE amplitude (DRVH Vp-p) and calculate ClampG = 100 × (1+(DRVPH - BRTPL)/DRVH).	Brightness: 0000000 Contrast: 1111111 DCREST = 00 BLK.ST.DEF = 1 WPL = 0
Sharpness variable range (PAL)	Sharp32T2	17	L-CW	With the input signal's continuous wave = 2.7MHz, measure the output signal's continuous wave amplitude (F02S32 Vp-p). Calculate Sharp32T3 = 20Log (F02S32/PEAKDC).	Filter Sys:0010 Sharpness: 100000
(max)	Sharp63T2	17	L-CW	With the input signal's continuous wave = 3MHz, measure the output signal's continuous wave amplitude (F02S63 Vp-p). Calculate Sharp63T2 = 20Log (F02S63/PEAKDC).	Filter Sys:0010 Sharpness: 111111
(min)	Sharp0T2	17	L-CW	With the input signal's continuous wave = 3MHz, measure the output signal's continuous wave amplitude (F02S0 Vp-p). Calculate Sharp0T2 = 20Log (F02S0/PEAKDC).	Filter Sys:0010 Sharpness: 000000

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Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Y gamma effective point1	YG1	17	L-100	Measure the output amplitude (0 to 100 IR) when the Y gamma is 0 (GAM0). Then set Y gamma to 1 and measure the output amplitude (0 to 100 IR) again (GAM1). Calculate YG1 = (GAM1/GAM0) × 100.	Y GAMMA = 1
Y gamma effective point12	YG2	17	L-100	Measure the output amplitude (0 to 100 IR) when the Y gamma is 0 (GAM0). Then set Y gamma to 2 and measure the output amplitude (0 to 100 IR) again (GAM2). Calculate YG2 = (GAM2/GAM0) × 100.	Y GAMMA = 2
Y gamma effective point1	YG3	17	L-100	Measure the output amplitude (0 to 100 IR) when the Y gamma is 0 (GAM0). Then set Y gamma to 3 and measure the output amplitude (0 to 100 IR) again (GAM3). Calculate YG3 = (GAM3/GAM0) × 100.	Y GAMMA = 3
Horizontal/vertical blanking output level	RGBBLK	17	L-100	Measure the DC level (RGBBLK V) for the output signal's blanking period.	
[OSD block]				Bus control bit conditions: Contrast = 63, Brightness = 63	Contrast: 0111111 Brightness: 0111111
OSD Fast SW threshold	FSTH	17	L-0 O-2	Apply voltage to pin 15 and measure the voltage at pin 15 at the point where the output signal switches to the OSD signal.	Pin 14A: O-2 applied
OSD output level	OSDH	17	L-50	Measure the output signal's 50IRE amplitude (CNTCB Vp-p).	Osd cont = 0111111 Digital osd = 1
			L-0 O-2	Measure the OSD output amplitude (OSDHB Vp-p). Calculate OSDH = 50 × (OSDHB/CNTCB)	Pin 15: 3.5V Pin 14A: O-2 applied
[Y output block] (Cutoff, drive block)				Bus control bit conditions: Contrast = 127	Contrast: 1111111
Brightness control (normal)	BRT63	17	L-0	Measure the 0IRE DC levels of the respective output signals of Y output (17)	Brightness: 01111111
Brightness control (normal-H)	BRT63H	17	L-0	Measure the 0IRE DC level of the output Signal of Y output (17) and assign the Measured value to BRTPC.	Brightness: 0111111 Sub Bias: 1111111
Brightness control (max)	BRT127	17	L-0	Measure the 0IRE DC level of the output Signal of Y output (17) and assign the Measured value to BRTPH. Calculate BRT127 = 50×(BRTPH-BRTPC)/CNTHB.	Brightness: 1111111 Sub Bias: 1111111
Brightness control (min)	BRT0	17	L-0	Measure the 0IRE DC level of the output Signal of Y output (17) and assign the Measured value to BRTPL. Calculate BRT0 = 50× (BRTPL-BRTPC)/CNTHB.	Brightness: 0000000 Sub Bias: 1111111
Bright control resolution	Vsiassns	17	L-50	Measure the 0IRE DC levels (BTPM V) of the respective output signals of Y output (17). Vbiassns = (BRTPH-BTPM)/127	Brightness: 0000000 Sub Bias: 1111111
Sub-bias control resolution	Vsbiassns	17	L-50	Measure the 0IRE DC levels (SBTPM V) of the respective output signals of Y output (17). Vsbiassns = (BRTPCH-SBTPM)/127	Brightness: 0111111 Sub Bias: 0000000

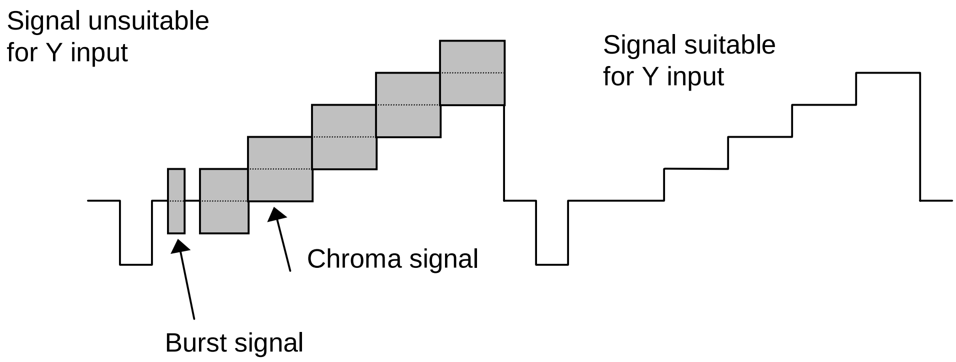
Deflection Block   Input Signals

Unless otherwise specified, the following conditions apply when each measurement is made.

1. VIF, SIF blocks: No signal
2. C input: No. signal
3. Sync input: A horizontal/vertical composite sync signal

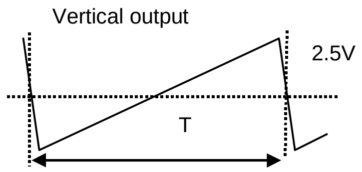
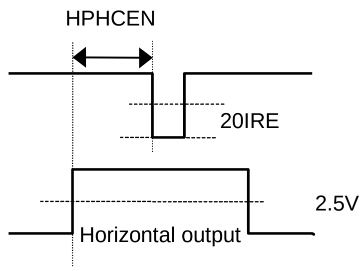
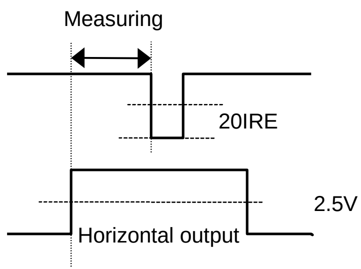
PAL: 43IRE, horizontal sync signal (15.625kHz) and vertical sync signal (50kHz)
NTSC: 40IRE, horizontal sync signal (15.734264kHz) and vertical sync signal (59.94kHz)

Note: No burst signal, chroma signal shall exist below the pedestal level.



4. Bus control conditions: Initial conditions unless otherwise specified.
5. The delay time from the rise of the horizontal output (pin 22 output) to the fall of the FBP IN (pin 23 input) is 9µs.
6. Pin 13 (vertical size correction circuit input terminal) is connected to V_{CC} (5.0V).

Deflection Block   Test Conditions

Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal free-running frequency	fH	22	Y IN: No signal	Connect a frequency counter to the output of pin 22 (H out) and measure the horizontal free-running frequency.	
Horizontal output pulse length	Hduty	22	Y IN: Horizontal/ vertical sync signal PAL	Measure the voltage for the pin 22 horizontal output pulse's low-level period.	
Horizontal output pulse saturation voltage	V Hsat	22	Y IN: Horizontal/ vertical sync signal PAL	Measure the voltage for the pin 22 horizontal output pulse's low-level period.	
Vertical free-running period 50 (PAL) Vertical free-running period 60 (NTSC)	VFR50 VFR60	18	Y IN: No signal	Measure the vertical output period T at pin 18 T×15.625kHz (PAL) T×15.734kHz (NTSC) 	CDMODE: 001 (PAL) CDMODE: 002 (NTSC)
Horizontal output pulse	HPHCEN (PAL) (NTSC)	22 28	Y IN: Horizontal/ vertical sync signal PAL NTSC	Measure the delay time from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal. 	
Horizontal position adjustment range	HPHrange	22 28	Y IN: Horizontal/ vertical sync signal PAL	With H PHASE: 0 and 31, measure the delay time from the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the difference from H PHCEN. 	H PHASE: 00000 H PHASE: 11111

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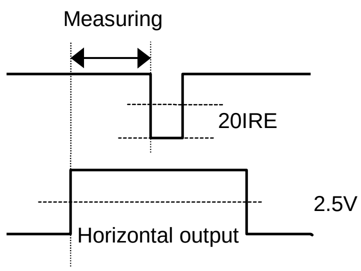
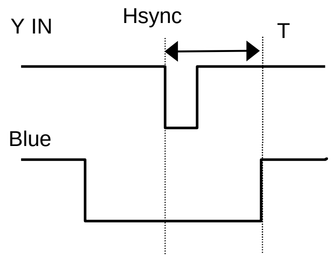
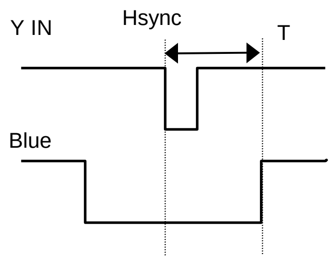
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal position adjustment maximum variable width	HPHstep	22 28	Y IN: Horizontal/ vertical sync signal PAL	With H PHASE: 0 to 31 varied, measure the delay time from to the rise of the pin 22 horizontal output pulse to the fall of the Y IN horizontal sync signal and calculate the variation at each step. Retrieve data for maximum variation.  	H PHASE: 00000 to H PHASE: 11111
Horizontal blanking left variable range@0	BLKL0	22 28	Y IN: Horizontal/ vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 28 Y IN to the left end of blanking at pin 17 BlueOUT with BLKL = 000.  	BLKL: 000
Horizontal blanking left variable range@7	BLKL7	17 28	Y IN: Horizontal/ vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 28 Y IN to the left end of blanking at pin 17 BlueOUT with BLKL = 111.  	BLKL:111

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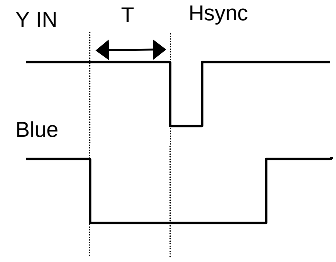
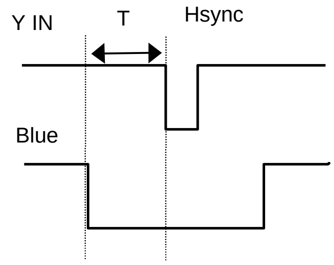
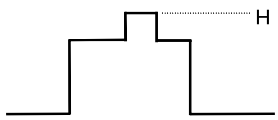
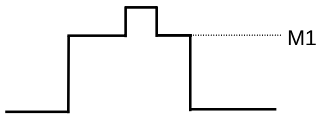
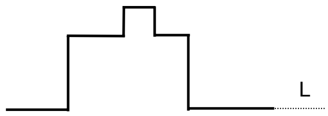
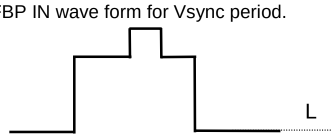
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Horizontal blanking right variable range@0	BLKR0	17 28	Y IN: Horizontal/ vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 28 Y IN to the left end of blanking at pin 17 BlueOUT with BLKR = 000.  	BLKR:000
Horizontal blanking right variable range@7	BLKR7	17 28	Y IN: Horizontal/ vertical sync signal PAL	Measure the time T from the left end of Hsync at pin 28 Y IN to the left end of blanking at pin 17 BlueOUT with BLKR = 111.  	BLKR:111
Sand castle pulse crest value H	SANDH	23	Y IN: Horizontal/ vertical sync signal PAL	Measure the supply voltage at point H of the pin 23 FBP IN wave form for Hsync period.  	
Sand castle pulse crest value M1	SANDM1	23	Y IN: Horizontal/ vertical sync signal PAL	Measure the supply voltage at point M1 of the pin 23 FBP IN wave form for Hsync period.  	
Sand castle pulse crest value L	SANDL	23	Y IN: Horizontal/ vertical sync signal PAL	Measure the supply voltage at point L of the pin 23 FBP IN wave form for Hsync period.  	
Sand castle pulse crest value M2	SANDM2	23	Y IN: Horizontal/ vertical sync signal PAL	Measure the supply voltage at point M2 of the pin 23 FBP IN wave form for Vsync period.  	

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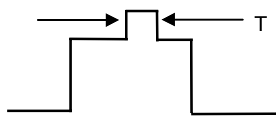
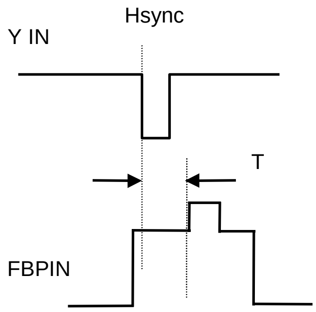
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Burst gate pulse length	BGPWD	23	Y IN: Horizontal/ vertical sync signal PAL	Measure the BGP width T of the pin 28 FBP IN wave form for Hsync period. 	
Burst gate pulse I phase	BGPPH	23 42	Y IN: Horizontal/ vertical sync signal PAL	Measure the time from the left end of Hsync at pin 42 Y IN to the left end of the pin 23 FBP IN wave form for Hsync period. 	
Horizontal output stop voltage	Hstop	20 22	Y IN: Horizontal/ vertical sync signal	Decrease the current from a source connected to pin 20 and measure the pin 20 voltage at which HOUT stops.	

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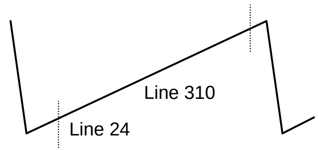
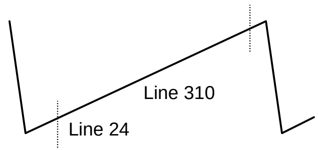
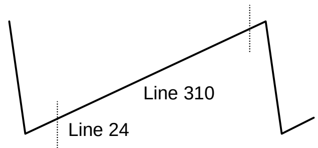
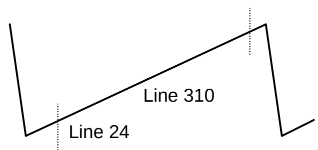
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
<Vertical screen size correction>					
Vertical ramp output Amplitude PAL@64 NTSC@64	Vspal64 Vsnt64	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 24 (22:NTSC) and line 310 (262:NTSC). Calculate as follows: Vspal64 = Vline310-Vline24 Vsnt64 = Vline262-Vline22 Vertical ramp output 	
Vertical ramp output amplitude PAL@0 NTSC@0	Vspal0 Vsnt0	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 24 (22:NTSC) and line 310 (262:NTSC). Calculate as follows: Vspal0 = Vline310-Vline24 Vsnt0 = Vline262-Vline22 Vertical ramp output 	VSIZE: 0000000
Vertical ramp output amplitude PAL@127 NTSC@127	Vspal127 Vsnt127	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 24 (22: NTSC) and line 310 (262: NTSC). Calculate as follows: Vspal27 = Vline310-Vline24 Vsnt127 = Vline262-Vline22 Vertical ramp output 	VSIZE: 1111111
<High-voltage dependent vertical size correction>					
Vertical size correction@0	Vsizecomp	18	Y IN: Horizontal/ vertical sync signal PAL	Monitor the pin 18 vertical ramp output and measure the voltage at the line 24 and line 310 with VCOMP = 000. Calculate as follows: Va = Vline310-Vline24 Apply 4.1V to pin 13 and measure the voltage at the line 24 and line 310 again. Calculate as follows: Va = Vline310-Vline24 Calculate as follows: Vsizecomp = Vb/Va Vertical ramp output 	VCOMP: 000

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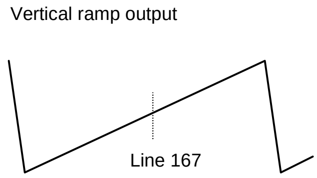
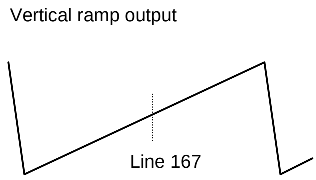
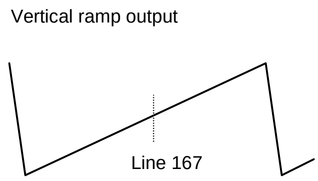
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
<Vertical screen position adjustment>					
Vertical ramp DC voltage PAL@32 NTSC@32	Vdcpal32 Vdcnt32	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 167. (PAL) Monitor the pin 18 vertical ramp output and measure the voltage at line 142. (NTSC) 	
Vertical ramp DC voltage PAL@0 NTSC@0	Vdcpal0 Vdcnt0	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 167. (PAL) Monitor the pin 18 vertical ramp output and measure the voltage at line 142. (NTSC) 	VDC: 000000
Vertical ramp DC voltage PAL@63 NTSC@63	Vdcpal63 Vdcnt63	18	Y IN: Horizontal/ vertical sync signal PAL NTSC	Monitor the pin 18 vertical ramp output and measure the voltage at line 167. (PAL) Monitor the pin 18 vertical ramp output and measure the voltage at line 142. (NTSC) 	VDC: 111111

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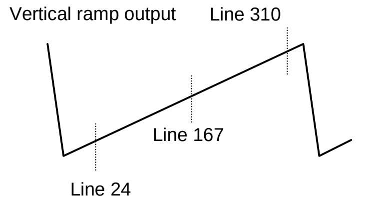
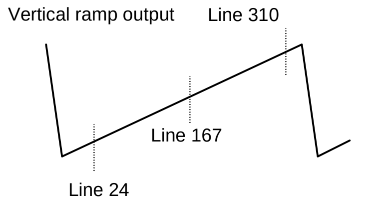
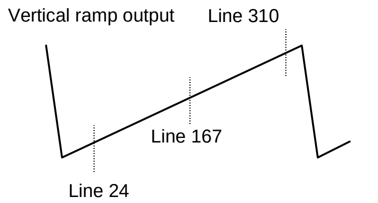
Input signal	Symbol	Test point	Input signal	Test method	Bus conditions
Vertical linearity@16	Vlin16	18	Y IN: Horizontal/ vertical sync signal PAL	Monitor the pin 18 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin16 = (Vb-Va)/(Vc-Vb) 	
Vertical linearity@0	Vlin0	18	Y IN: Horizontal/ vertical sync signal PAL	Monitor the pin 18 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin0 = (Vb-Va)/(Vc-Vb) 	VLIN: 00000
Vertical linearity@31	Vlin31	18	Y IN: Horizontal/ vertical sync signal PAL	Monitor the pin 18 vertical ramp output and measure the voltage at line 24, line 167 and 310. Assign the respective measured values to Va, Vb and Vc. Calculate as follows: Vlin31 = (Vb-Va)/(Vc-Vb) 	VLIN: 11111

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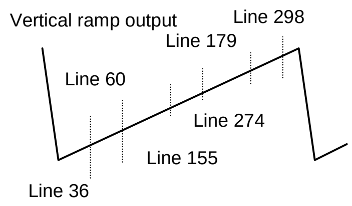
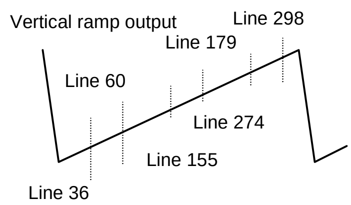
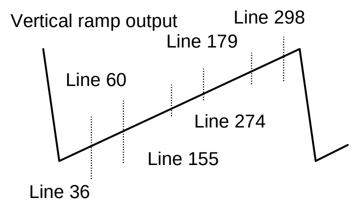
<table>
<tr><th>Input signal</th><th>Symbol</th><th>Test point</th><th>Input signal</th><th>Test method</th><th>Bus conditions</th></tr>
<tr><td>Vertical S-shaped correction @16</td><td>VScor16</td><td>18</td><td>Y IN:
Horizontal/
vertical sync signal
PAL</td><td>Monitor the pin 18 vertical ramp output and measure the voltage at line 36, line 60, line 155, line 179, line 274 and 298. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows:
VScor16 = 0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc)

</td><td>VS: 10000</td></tr>
<tr><td>Vertical S-shaped correction @0</td><td>VScor0</td><td>18</td><td>Y IN:
Horizontal/
vertical sync signal
PAL</td><td>Monitor the pin 18 vertical ramp output and measure the voltage at the line 36, line 60, line 155, line 179, line 274 and line 298 with VSC = 00000.
Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows:
VScor0 = 0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc)

</td><td></td></tr>
<tr><td>Vertical S-shaped correction @31</td><td>VScor31</td><td>18</td><td>Y IN:
Horizontal/
vertical sync signal
PAL</td><td>Monitor the pin 18 vertical ramp output and measure the voltage at line 36, line 60, line 155, line 179, line 274 and 298. Assign the respective measured values to Va, Vb, Vc, Vd, Ve and Vf. Calculate as follows:
VScor16 = 0.5((Vb-Va)+(Vf-Ve))/ (Vd-Vc)

</td><td>VSC: 11111</td></tr>
</table>

Control Register Bit Allocation Map

Control Register Bit Allocations (continued)								
Sub Address	MSB				DATA BITS			LSB
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7
00010000	OSD Cnt.Test	OSD Contrast						
	0	1	0	0	0	0	0	0
10001	Coring Gain(W/Defeat)		Sharpness					
	0	0	0	0	0	0	0	0
10010	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10011	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10100	*	Trap Test			Filter.Sys			
	(0)	1	0	0	0	0	1	0
10101	Gray Mode	Cross B/W		*	*	*	*	*
	0	0	0	(0)	(0)	(0)	(0)	(0)
10110	VBLK SW	FBPBLK. SW	*	Y_APF	Pre/Over-shoot adj.		*	*
	0	1	(0)	0	0	0	(0)	(0)
10111	Y Gamma Start		*	*	*	*	*	*
	0	0	(0)	(0)	(0)	(0)	(0)	(0)
11000	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11001	Cont. Test	Digital OSD	Brt.Abl. Def	Mid.Stp.Def	RGB Temp SW	Bright.Abl.Threshold		
	0	0	0	0	0	1	0	0
11010	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11011	*	*	*	*	*	*	*	*
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11100	*	Volume						
	(0)	0	0	0	0	0	0	0
11101	OVER. MOD.SW	VOL.FIL	RF.AGC					
	0	0	1	0	0	0	0	0
11110	FM.Mute	deem.TC	VIF.Sys.SW		SIF.Sys.SW		FM.Gain	IF.AGC
	0	0	0	1	0	1	0	0
11111	VIDEO.LEVEL			*	*	*	*	*
	1	0	0	(0)	(0)	(0)	(0)	(0)

(Bits are transmitted in this order.)

Control Register Truth Table

Register Name	0 HEX	1 HEX	2 HEX	3 HEX
T.Disable	Tset Enable	Test Disable		
AFC gain&gate	Auto (Gain)	Gain:Fast		
	Auto (Gate)	Non-Gate		
V Reset Timing	Normal	1/4H Shift		
Audio.Mute	Active	Mute		
Video.Mute	Active	Mute		
Sync.Kill	Sync active	Sync killed		
Vsepup	normal	Vsepup		
V.KILL	Vrt active	Vrt killed		
Vertical Test	Normal	Vrt S Corr	Vrt Lin	Vrt Size
Drive.Test	Normal	Test Mode		
Half Tone	Min (Dark)	→	→	Max
Half Tone Def	Half Tone on	Half Tone off		
Blank.Def	Blanking	No Blank		
S.TRAP.SW	Bypass ON	Bypass OFF		
OSD Cnt.Test	Normal	Test Mode		
Coring Gain(w/Defeat)	Defeat	Min	→	Max
Color.Test	Normal	Test Mode		
Video.SW	Internal Mode	External Mode		
Gray Mode	Normal	Gray OSD		
Cross B/W	Normal	Black	White	Cross
G-Y Angle	240deg	253deg		
VBLK SW	24H to 262H (NTSC)	29H to 256H (NTSC)		
	25H to 309H (PAL)	30H to 304H (PAL)		
FBPBLK.SW	FBP not or	FBP or		
Y APF	Y Trap	Y APF		
Pre/Over-shoot adj.	Normal	+10ns	+20ns	+30ns
Y Gamma Start	Y Gamma off	Min	→	Max
Digital OSD	Analogue	Digital		
Brt.ABL.Def	Brt ABL On	Brt ABL Off		
Mid.Stp.Def	Mid Stp On	Mid Stp Off		
RGB Temp SW	-1Vbe	Flat		
OVER.MOD.(circuit)SW	circuit OFF	circuit ON		
VOL.FIL	Normal	Filte OFF		
FM.Mute	Active	Mute		
de-em TC.	50µs	75µs		
VIF.Sys.SW	38.0MHz	38.9MHz	45.75MHz	39.5MHz
FM Gain	50kHz dev.	25kHz dev		
IF.AGC	AGC active	AGC defeat		
Pre/Over SW	Pre-shoot Adj.	Over-shoot Adj.		
Hlock.Vdet	Individual Operation	Normal		
VIDEO.LEVEL.OFFSET	direction: Minus	Center		direction: Plus

Control Register Truth Table

COUNT DOWN MODE

	50Hz/60Hz MODE	Standard/Non-Standard MODE
0 HEX	Auto	Auto
1 HEX	50Hz	Auto
2 HEX	60Hz	Auto
3 HEX	Auto	Auto
4 HEX	Auto	Non-Standard
5 HEX	50Hz	Non-Standard
6 HEX	60Hz	Non-Standard
7 HEX	Auto	Non-Standard

Filter System

	Y Filter	Chroma Filter
0 HEX	3.58MHz Trap	Peaked 3.58MHz BPF
1 HEX	3.58MHz Trap	Symmetrical 3.58MHz BPF
2 HEX	4.43MHz Trap	Peaked 4.43MHz BPF
3 HEX	4.43MHz Trap	Symmetrical 4.43MHz BPF
4 HEX	6.0MHz Trap	Peaked 3.58MHz BPF
5 HEX	6.0MHz Trap	Symmetrical 3.58MHz BPF
6 HEX	6.0MHz Trap	Peaked 4.43MHz BPF
7 HEX	6.0MHz Trap	Symmetrical 4.43MHz BPF
8-15HEX	4.286MHz Trap	Symmetrical 4.43MHz BPF

Snd.Trap & FM.Det

A2.SW	SIF.Sys.SW	Snd.Trap	FM.det
0 HEX	0 HEX	4.5MHz	4.5MHz
	1 HEX	5.5MHz	5.5MHz
	2 HEX	6.0MHz	6.0MHz
	3 HEX	6.5MHz	6.5MHz
1 HEX	0 HEX	-----------	-----------
	1 HEX	5.5NHz	5.74MHz
	2 HEX	-----------	-----------
	3 HEX	-----------	-----------

Audio Monitor Output

A.MONI.SW	AUDIO.SW	1pin Output	2pin Output
0 HEX	0 HEX	Internal	Internal
	1 HEX	External	
1 HEX	0 HEX	Internal	Internal
	1 HEX	External	External (before VOLUME)

Status Byte Truth Table

Register	0 HEX	1 HEX
RF.AGC	RF.AGC.OUT = "L"	RF.AGC.OUT = "H"
IF.LOCK	IF.PLL Lock	IF.PLL Unlock
V.TRI	V.Triger Undetected	V.Triger Detected
50/60	50	60
ST/NONST	Non-Standard	Standard

Initial Conditions

Initial Test Conditions	
Register Name	Value
T.Disable	1 HEX
AFC gain&gate	0 HEX
H.FREQ	3F HEX
V Reset Timing	0 HEX
Audio.Mute	0 HEX
Video.Mute	0 HEX
H.PHASE	10 HEX
Sync.Kill	0 HEX
V.SIZE	40 HEX
VSEPUP	0 HEX
V.KILL	0 HEX
V.POSI	20 HEX
H BLK L	4 HEX
H BLK R	4 HEX
V.LIN	10 HEX
V.SC	00 HEX
V.TEST	0 HEX
V.COMP	7 HEX
COUNT.DOWN.MODE	0 HEX
RGB Test 4	0 HEX
Half Tone	1 HEX
Half Tone Def	1 HEX
A2 SW	0 HEX
Blank.Def	0 HEX
Sub.Bias	40 HEX
A.MONI.SW	0 HEX
Bright	40 HEX
S.TRAP.SW	1 HEX
Contrast	40 HEX
OSD Cnt.Test	0 HEX
OSD Contrast	0 HEX

Initial Test Conditions (continued)	
Register Name	Value
VBLK SW	0 HEX
FBPBLK.SW	1 HEX
Y_APF	0 HEX
Pre/Over-shoot Adj.	0 HEX
Y Gamma	0 HEX
Digitsl OSD	0 HEX
Brt.Abl.Def	0 HEX
Mid.Stp.Def	0 HEX
RGB Temp SW	0 HEX
Bright.Abl.Threshold	4 HEX
Volume	00 HEX
OVER.MOD.SW	0 HEX
VOL.FIL	0 HEX
RF.AGC	20 HEX
FM.Mute	0 HEX
deem.TC	0 HEX
VIF.Sys.SW	1 HEX
SIF.Sys.SW	1 HEX
FM.Gain	0 HEX
IF.AGC	0 HEX
VIDEO.LEVEL	4 HEX
Pre/Over SW	0 HEX
H lock.Vdet	0 HEX
VIDEO.LEVEL.OFFSET	1 HEX
IF.TEST1	0 HEX
OVER.MOD.LEVEL	8 HEX
Coring Gain (w/Defeat)	0 HEX
Sharpness	00 HEX
Trap.Test	4 HEX
Filter.Sys	2 HEX
Gray Mode	0 HEX
Cross B/W	0 HEX

Control Register Descriptions

Register Name	Bits	General Description
T Disable	1	Disable the Test SW & enable Audio/Video Mute SW
AFC Gain & gate	1	Select horizontal first loop gain & H-sync gating on/off
H Freq.	6	Align ES Sample horizontal frequency
V Reset Timing	1	Select Vertical Reset Timing
Audio Mute	1	Disable audio outputs
Video Mute	1	Disable video outputs
H PHASE	5	Align sync to flyback phase
Sync Kill	1	Force free-run mode
Vertical Size	7	Align vertical amplitude
Vsep.up	1	Select vertical sync. separation sensitivity
Vertical Kill	1	Disable vertical output
V POSI (Vertical DC)	6	Align vertical DC bias
H BLK L	3	H-Blanking Control (Left side of the screen)
H BLK R	3	H-Blanking Control (Right side of the screen)
V LIN (Vertical Linearity)	5	Align vertical linearity
Vertical S-Correction	5	Align vertical S-correction
Vertical Test	2	Select vertical DAC test modes
Vertical Size Compensation	3	Align vertical size compensation
Count Down Mode	1	Select vertical countdown mode
Half Tone	2	Adjust half tone DC level
Half Tone Defeat	1	Half tone defeat SW
A2.SW	1	Select 5.74MHz FM.Det
Blank Def	1	Disable RGB output blanking
Sub Bias	7	Align common RGB DC level
A.MONI.SW	1	Select FM Output/Selected Audio Output
Brightness Control	7	Customer brightness control
S.TRAP.SW	1	Select Snd Trap bypass
Contrast Control	7	Customer contrast control
OSD Contrast Test	1	Enable OSD Contrast DAC test mode
OSD Contrast Control	2	Align OSD AC level
Coring Gain Select (with Defeat)	2	Select Coring Gain (0hex: Defeat)
Sharpness Control	6	Customer sharpness control
Trap.Test	3	Trap Test
Filter System	3	Select Y/C Filter mode
Gray Mode	1	OSD Gray Tone Enable
Cross B/W	2	Service Test Mode (normal/Black/White/Cross)
Vertical Blanking SW	1	Select VBLK Period
FBPBLK.SW	1	Enable RGB Blanking or FBP
Y APF Enable SW	1	Select the frequency caracteristic of 3.58MHzTrap. It is useful for 3.58MHzTrap or APF
Pre/Over-shoot Adjustmant	2	Select Pre-shoot Width
Y Gamma Start	2	Enable luminance coring
DC Restoration Select	2	Select Luma DC Restoration
Cont Test	1	Enable contrast DAC test mode
Digital OSD SW	1	Select Digital/Analogue OSD
Bright ABL Defeat	1	Disable brightness ABL
Bright Mid Stop Defeat	1	Disable brightness mid stop
RGB Temp SW	1	Select temprature caracteristic of RGB Output
Bright ABL Threshold	3	Align brightness ABL threshold
Volume Control	7	Customer volume control
OVER.MOD.SW	1	Select overmodulation circuit ON/OFF

Continued on next page.

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Register Name	Bits	General Description
Volume Filter Defeat	1	Disable volume DAC filter
RF AGC Delay	6	Align RF AGC threshold
FM Mute	1	Disable FM outputs
de-em TC.	1	Select de-emphasis Time Constant
VIF System SW	2	Select 38.0/38.9/39.5/45.75
SIF System SW	2	Select 4.5/5.5/6.0/6.5
FM Gain	1	Select FM Output Level
IF AGC Defeat	1	Disable IF and RF AGC
Video Level	3	Align IF video level
FM Level	5	Align FM output level
Pre/Over SW	1	Select control for Pre/Over-shoot Adjustmant
H Lock Vdet	1	Select vertical sync. Operation
VIDEO.LEVEL.OFFSET	2	Align IF video level
IF TEST1	1	Select test modes
OVER.MOD.LEVEL	4	Align overmodulation performance

Read Status Description

RF.AGC	0: RF AGC = low, 1: RF AGC = high. See the separately provided documentation (Application Note) for details.
IF.LOCK	0: IF.PLL = Locked, 1: IF.PLL = Unlocked
V.TRI	Returns the output of the VCD internal vertical trigger detection circuit to the bus. The state of the internal memory is updated every vertical period. 1HEX: Detected
50/60	Returns the output of the VCD internal 50/60 Hz detection output to the bus.
ST/NONST	Returns to the bus whether a standard (262.5H) VCD or a nonstandard internal vertical trigger detection circuit output VCD is used.
	Returns the FF output determined by the VCD internal mode in real time. 1HEX: Standard
H.Lock	Performs FBP and Hsync phase detection, integrates that output, and detects at a point about 40H after the HVCO locks.
	Returns, in real time, the state with respect to bus reads. 1Hex: Locked